

IN THE CLAIMS:

The following listing of claims replaces all listing of claims in this application.

Claim 1 (Currently Amended): An integrated circuit comprising:

- a plurality of computational elements;

- a first and a second processing node each having a core processor with a common architecture, wherein the common architecture is configurable in response to a first configuration command to be a control node adapted to control an interconnection of said computational elements to perform a selected task and configurable in response to a second configuration command to be a programmable scalar node (PSN) adapted to perform a computational application;

- a first memory associated with said first processing node;

- a second memory associated with said second processing node, each of said first and second memories including at least one of a data cache and an instruction cache of sufficient capacity to store instructions and data necessary to implement a plurality of algorithms;

- a first interface coupling said core processor of said first processing node to said first memory and to said computational elements;

- a second interface coupling said core processor of said second processing node to said second memory and to said computational elements, the first interface and the second interface having the same architecture; and

- a third processing node coupled to each of the first and second processing nodes and comprising a core processor with a common architecture, wherein the common architecture is configurable in response to a first configuration command to a control node adapted to control an interconnection of said computational elements to perform a selected task and configurable in response to a second configuration command to a programmable scalar node (PSN) adapted to perform a computational application and being configured to run boot code, operating system code and application code and further configured to adapt each of the first and second processing nodes to perform the computational application in response to the first and second configuration commands.

Claim 2 (Original): The integrated circuit of claim 1 further comprising means for temporally adapting said second node and said computational elements to perform a selected function.

Claim 3 (Original): The integrated circuit of claim 2 wherein said temporal means further comprises executable code defining said selected function stored in at least said first memory.

Claim 4 (Original): The integrated circuit of claim 3 wherein said executable code is downloaded from the Internet by said first processing node.

Claim 5 (Original): The integrated circuit of claim 4 wherein said executable code comprises operating system code.

Claim 6 (Original): The integrated circuit of claim 5 wherein said first processing node initiates the temporal adaptation of said computational elements and said second processing node to perform said selected function.

Claim 7 (Previously Presented): The integrated circuit of claim 1 wherein said plurality of computational elements are adapted to form at least one arithmetic node, at least one of bit-manipulation node and at least one finite state machine nodes

Claim 8 (Previously Presented): The integrated circuit of claim 1 further comprising a plurality of said second processing nodes and an interconnection network, the plurality of said second processing nodes coupled through the interconnection network to said first processing node and plurality of computation elements.

Claim 9 (Currently Amended): An integrated circuit comprising:
a first node having:

a first core processing configurable in response to a first configuration signal to a controller node for execution of operating system code;

a first memory for storing operating system executable code;

means for transferring operating system executable code and data from said first memory to said first core processor;

a plurality of computational elements adapted to perform a selected function;

a second node having:

a second core processor having the same circuit architecture as the first core processor, the second core processor configurable into a RISC processor for execution of application code;

a second memory for storing application code;

means for transferring application code and data from said second memory to said second core processor;

an interconnection network coupling said controller node and said RISC processor to said ~~Plurality~~ plurality of computational elements to perform the selected ~~function~~ function;

a first interface coupling said first core processor to said interconnection network;

a second interface coupling said second core processor to said interconnection network, the first and second interfaces having a common interface architecture; and

a third processing node coupled to each of the first and second processing nodes and comprising a core processor with a common architecture, wherein the common architecture is configurable in response to a first configuration command to a control node adapted to control an interconnection of said computational elements to perform a selected task and configurable in response to a second configuration command to a programmable scalar node (PSN) adapted to perform a computational application and being configured to run boot code, operating system code and application code and further configured to adapt each of the first and second processing nodes to perform the computation application in response to the first and second configuration commands.

Claim 10 (Previously Presented): The integrated circuit of claim 9 wherein said first node further comprises a configuration register, said configuration register containing a

bit for determining whether said first node functions as the controller node or as a RISC processor.

Claim 11 (Previously Presented): The integrated circuit of claim 9 wherein said configuration register bit, when set, protects a portion of memory from access by said computational elements.

Claim 12 (Previously Presented): The integrated circuit of claim 9 further comprising a protected portion of memory accessible only to said controller node.

Claim 13 (Currently Amended): The integrated circuit of claim 9 wherein said first node and said second node further comprise:

- an interface comprising:

- a data distributor for receiving an input stream from an external source, said input stream having configuration information, application code or executable code;

- a hardware task manager for receiving configuration information from said data distributor;

- a DMA engine for receiving data and executable code from said data distributor;

- a controller for providing said interface access to a set of registers associated with the corresponding first or second core processor; and

- an interrupt controller for detecting an interrupt condition.

Claims 14-22 (Cancelled)

Claim 23 (Currently Amended): The integrated circuit of claim 1, wherein the third node ~~control node~~ is configured to change the interconnecting of said computational elements and said first and second processing nodes to define a second task to achieve a second function previously not available or existent.

Claim 24 (Cancelled)

Claim 25 (Previously Presented): The integrated circuit of claim 9, wherein the controller node is configured to change the interconnection network coupling said controller node to said computational elements to perform a second selected function previously not available or existent.

Claim 26 (New): The integrated circuit of claim 1, wherein the third node controls access to each of the first and second memories so that each of the first and second processing nodes can access only a second memory page within the memory.